



***Structured eASIC Ranked #1 Logic & Programmable Logic - Ultimate Product in a Survey of over 1,300 Engineers***

*In a study held by EE Times and eeProductCenter published on September 27 2004, Structured eASIC was ranked #1 on both "technical significance" and "likelihood of use" categories.*

At Electronica 2004 in Munich, on November 9-12, eASIC will introduce the test results of the first taped out Structured eASIC product – FA600. The test chips, fabricated by a European IDM partner at 0.13 micron process, were used to test functionality and characterize timing and power for the Structured eASIC device. The FA600 is the smallest member of the company's Structured eASIC product family. Structured eASIC products feature an innovative combination of FPGA-like flexibility and ASIC-like performance in a unique offering of NRE-free ASIC. The complete product family is scheduled for production release in Q1 2005.

**About eASIC**

eASIC® has developed a breakthrough Structured ASIC technology, protected by 10 issued US patents. The Structured eASIC technology was successfully proven in silicon and validated by customers.

eASIC Corporation is a privately held company, Venture Capital backed by Kleiner Perkins Caufield and Byers. Headquartered in San-Jose, California, eASIC was founded in 1999 by Zvi Or-Bach, the founder of Chip Express who is viewed by many as the "father of Structured ASIC technology". [www.eASIC.com](http://www.eASIC.com)

**Link to EE Times' Ultimate Products Supplement:**

<http://www.eeproductcenter.com/ultimate/default.html;jsessionid=KBFZIL41TMCTWQSNDBGCKHY>

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